Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method for synthesizing a circuit representation having initial unateness into a new circuit representation having greater unateness wherein the circuit has a function, the method comprising:

(i) partitioning the circuit representation to obtain a representation of at least one sub-circuit;

(ii) recursively decomposing the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit; and

(iii) merging the sum-of-products or product-of-sums representation into the circuit representation to form a new circuit representation having a unateness greater than the initial unateness while maintaining the function of the circuit substantially unchanged.

2. (original) The method of claim 1 additionally comprising repeating steps (i), (ii) and (iii) until a desired level of unateness for the new circuit representation has been achieved.

3. (original) The method of claim 1 wherein the sum-of-products or product-of-sums representation selected for each decomposition is the representation having fewer binate variables.

4. (original) The method of claim 1 additionally comprising merging common expressions of the sum-of-products or product-of-sums representations.

5. (original) The method of claim 4 wherein algebraic division is implemented to merge common unate expressions of the sum-of-products or product-of-sums representation.

6. (original) The method of claim 1 wherein the circuit is a digital circuit.

7. (original) The method of claim 1 wherein the representation of the at least one sub-circuit is highly unate.

8. (original) The method of claim 1 wherein a binary decision diagram is employed to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation.

9. (original) The method of claim 8 wherein the binary decision diagram is a zero-suppressed binary decision diagram.

10. (currently amended) A system for synthesizing a circuit representation having initial unateness into a new circuit representation having greater unateness wherein the circuit has a function, the system comprising a computing device configured to:

(i) receive input defining the circuit representation;

(ii) partition the circuit representation to obtain a representation of at least one sub-circuit;

(iii) recursively decompose the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit;

(iv) merge the sum-of-products or product-of-sums representation into the circuit representation to form the new circuit representation having a unateness greater than the initial unateness while maintaining the function of the circuit substantially unchanged; and

(v) output the new circuit representation.

11. (original) The system of claim 10 wherein the computing device is additionally configured to:

receive input defining a desired level of unateness for the new circuit representation; and

repeat steps (ii), (iii) and (iv) until the desired level of unateness is achieved.

12. (original) The system of claim 10 wherein the computing device is additionally configured to, for each decomposition, select the sum-of-products or product-of-sums representation having fewer binate variables.

13. (original) The system of claim 10 wherein the computing device is additionally configured to merge common expressions of the sum-of-products or product-of-sums representations.

14. (original) The system of claim 13 wherein the computing device is additionally configured to implement algebraic division to merge common expressions.

15. (original) The system of claim 10 wherein the circuit is a digital circuit.

16. (original) The system of claim 10 wherein the representation of the at least one sub-circuit is highly unate.

17. (original) The system of claim 10 wherein the computing device is additionally configured to employ a binary decision diagram to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation.

18. (original) The system of claim 17 wherein the binary decision diagram is a zero-suppressed binary decision diagram.

19. (original) The system of claim 10 wherein the circuit representation and the new circuit representation are input and output in a hardware description language.

20. (currently amended) A system for synthesizing a circuit representation having initial unateness into a new circuit representation having greater unateness wherein the circuit has a function, the system comprising:

(i) a means for receiving input defining the circuit representation;

(ii) a means for partitioning the circuit representation to obtain a representation of at least one sub-circuit;

(iii) a means for recursively decomposing the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit;

(iv) a means for merging the sum-of-products or product-of-sums representation into the circuit representation to form the new circuit representation having a unateness greater than the initial unateness while maintaining the function of the circuit substantially unchanged; and

(v) a means for outputting the new circuit representation.

21. (original) The system of claim 20 additionally comprising:

a means for receiving input defining a desired level of unateness for the new circuit representation; and

a means for repeating steps (ii), (iii) and (iv) until the desired level of unateness is achieved.

22. (original) The system of claim 20 additionally comprising a means for selecting, for each decomposition, the sum-of-products or product-of-sums representation having fewer binate variables.

23. (original) The system of claim 20 additionally comprising a means for merging common expressions of the sum-of-products or product-of-sums representations.

24. (original) The system of claim 20 additionally comprising a means for implementing algebraic division to merge common expressions.

25. (original) The system of claim 20 additionally comprising a means for partitioning the circuit representation such that the representation of the at least one sub-circuit is highly unate.

26. (original) The system of claim 20 additionally comprising a means for employing a binary decision diagram to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation.

27. (original) The system of claim 26 wherein the binary decision diagram is a zero-suppressed binary decision diagram.

28. (original) The system of claim 20 wherein the circuit representation and the new circuit representation are input and output in a hardware description language.

29. (currently amended) A computer-readable storage medium containing computer executable code for instructing one or more computers to:

(i) receive input defining a circuit representation <u>having initial unateness wherein the circuit has a function</u>;

(ii) partition the circuit representation to obtain a representation of at least one sub-circuit;

(iii) recursively decompose the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit;

(iv) merge the sum-of-products or product-of-sums representation into the circuit representation to form a new circuit representation <u>having a unateness greater than the initial unateness while maintaining the function of the circuit substantially unchanged</u>; and

(v) output the new circuit representation.

30. (original) The computer-readable storage medium of claim 29 wherein the computer executable code additionally instructs the computer(s) to:

receive input defining a desired level of unateness for the new circuit representation; and

repeat steps (ii), (iii) and (iv) until the desired level of unateness is achieved.

31. (original) The computer-readable storage medium of claim 29 wherein the computer executable code additionally instructs the computer(s) to, for each decomposition, select the sum-of-products or product-of-sums representation having fewer binate variables.

32. (original) The computer-readable storage medium of claim 29 wherein the computer executable code additionally instructs the computer(s) to merge common expressions of the sum-of-products or product-of-sums representations.

33. (original) The computer-readable storage medium of claim 32 wherein the computer executable code additionally instructs the computer(s) to implement algebraic division to merge common expressions.

34. (original) The computer-readable storage medium of claim 29 wherein the circuit is a digital circuit.

35. (original) The computer-readable storage medium of claim 29 wherein the representation of the at least one sub-circuit is highly unate.

36. (original) The computer-readable storage medium of claim 29 wherein the computer executable code additionally instructs the computer(s) to employ a binary decision diagram to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation.

37. (original) The computer-readable storage medium of claim 36 wherein the binary decision diagram is a zero-suppressed binary decision diagram.

38. (original) The computer-readable storage medium of claim 29 wherein the circuit representation and the new circuit representation are input and output in a hardware description language.

Add new claims 39-45.

39. (new) A method for synthesizing an original circuit representation Gc into a new circuit Gn having greater unateness, the method comprising:

(i) calculating the binateness of each node in the circuit Gc by recursively computing the number of paths from every primary input of Gc with even and odd number of inversion parities;

(ii) partitioning the circuit representation into sub-circuit1 and sub-circuit2, wherein sub-circuit1 has minimal binateness calculated by step (i), while meeting a specified limit on the size of the sub-circuit1;

(iii) decomposing sub-circuit1 partitioned by step (ii) into unate sub-functions of at least 2 levels by recursively applying a unate decomposition procedure that splits a function into a unate sub-function and a binate sub-function in a way that maximizes the unateness of both sub-functions;

(iv) maximizing the unateness of the result of the unate decomposition by simultaneously constructing AND-decomposition and OR-decomposition whose terms are subsequently split into unate terms and binate terms by eliminating the binate terms that maximize the combined binateness of all the resulting terms;

(v) breaking the final decomposed sub-functions into unate parent function block B2 and unate child function block B1, and merging block B2 into sub-circuit2 to construct an intermediate circuit, and merging block B1 into the new circuit Gn; and

(vi) repeating steps (i), (ii), (iii), (iv) and (v) with the intermediate circuit and replacing the circuit Gc until the original circuit is completely transformed into a new circuit.

40. (new) The method of claim 39, wherein the number Pe of paths with even inversion parity and the number Po of paths with odd inversion parity from a primary input Si to an internal node Nc of the circuit are computed as follows:

calculating by recursively adding to Pe the number of paths with even inversion parity from Si to each node Ni within a fan-in cone of the said node Nc, if the inversion parity from Ni to Nc is even, and otherwise by recursively adding to Pe the number of paths with odd inversion parity from Si to each node Ni within the fan-in cone of the said node Nc; and

calculating by recursively adding to Po the number of paths with odd inversion parity from Si to each node Ni within the fan-in cone of the said node Nc, if the inversion parity from Ni to Nc is even, and otherwise by recursively adding to Po the number of paths with even inversion parity from Si to each node Ni within the fan-in cone of the said node Nc.

41. (new) The method of claim 40, further comprising calculating the binateness of each node Nc in the circuit by adding all binateness Bi of Nc with respect to each primary input Si, where the binateness Bi is defined as 0 if Pe of Nc with respect to Si is 0, or if Po of Nc with respect to Si is 0, and otherwise, the binateness Bi is defined as 1.

42. (new) The method of claim 39, wherein sub-circuit1 is constructed by repeatedly moving from sub-circuit2 to sub-circuit1 the node of the smallest binateness until the size of sub-circuit1 is not less than a specified threshold, which can be, but is not limited to, the number of inputs and outputs of sub-circuit1.

43. (new) The method of claim 39, wherein the maximum unateness is achieved by minimizing the binateness of the binate sub-function obtained as a result of the step of decomprising wherein the binateness of a function is defined as the sum of the binateness of all the terms in the function.

44. (new) The method of claim 39, further comprising selecting the AND-decomposition or OR-decomposition that leads to a unate decomposition having a binate sub-function of less binateness, and replacing the corresponding node of the original function of sub-circuit1 by the selected decomposition.

45. (new) The method of claim 44, wherein the AND-decompositions and OR-decompositions are constructed by:

(vii) representing each output node function of sub-circuit1 by a sum-of-products form, and selecting terms containing binate literals that, when eliminated, lead to a remainder function of minimal binateness, wherein the remainder function is constructed by means of cofactoring the sum-of-products form with respect to each binate literal;

(viii) repeating the step of repeating with the remainder function replacing the output function until the binateness of the remainder function is not greater than a specified threshold, and defining the final remainder function as the unate sub-function and defining the original output function excluding the terms of the unate sub-function as the binate sub-function;

(ix) repeating (vii) and (viii) with a product-of sums form replacing the sum-of-products form;

(x) selecting the AND-decomposition constructed by (vii) to (viii), or the OR-decomposition constructed by (ix), whichever generates the binate sub-function of the smaller binateness, and replacing the corresponding output function by the selected decomposition; and

(xi) repeating (vii) to (x) for every output node function and internal node function of sub-circuit1, that are binate, and eliminating the same sub-functions that exist in the decompositions of 2 or more output node functions by applying sharing operations such as, while not limited to, division operations using both unate-functions and binate sub-functions as divisors.